ADC and DAC

1. ADC involves two hazards that may prevent reconstruction of the input signal. What are they? Which is additive? Which is possible to overcome and how?

2. True or False (and why):

    a. S/H circuit causes quantization.
    b. Output of S/H stage is a discrete signal.
    c. We can completely remove quantization effect on a general signal.
    d. Some signals are not affected by quantization.

3. What are the factors affecting the noise level caused by quantization? What are the factors controlling the effect of sampling?
4. If the maximum amplitude of a signal is 8 volts and an 8-bits ADC was used to convert it into a digital form:
    a. What is the RMS of the noise introduced due to quantization?
    b. If the ADC cannot approximate the signal level by the nearest digital level but by the largest level equal to or less than it (truncation rather than rounding). What is the RMS of the noise introduced? For example in this system if the input is 4.9 and the nearest levels are either 4 or 5 it will approximate the input with 4.
    c. If the input signal had an additive noise component of 2mV RMS. What is the RMS of the total noise in the signal after quantization?
    d. How many bits are needed to reduce the effect of quantization to half?
5. A signal passes through systems A, B, C, and D with bandwidths 100MHz, 1GHz, 100KHz, 450Hz. What is the minimum sampling rate required to prevent aliasing when converting this signal to a digital form?
6. Why do we need an antialiasing filter even if we are not interested in signals over the Nyquest frequency?
7. A system is expected to process only triangle signals. Does it need a dithering circuit? What if it is expected to process square signals with a period of few hundred sampling times?
8. A signal was converted to a digital form using a sampling frequency of 100KHz What will be the low frequency alias (and the phase shift if any) for the following frequencies:
    a. 1MHz
    b. 3.454MHz
    c. 340KHz
    d. 45KHz
    e. 421KHz