EC325 Microprocessors
x86 Basic Architecture

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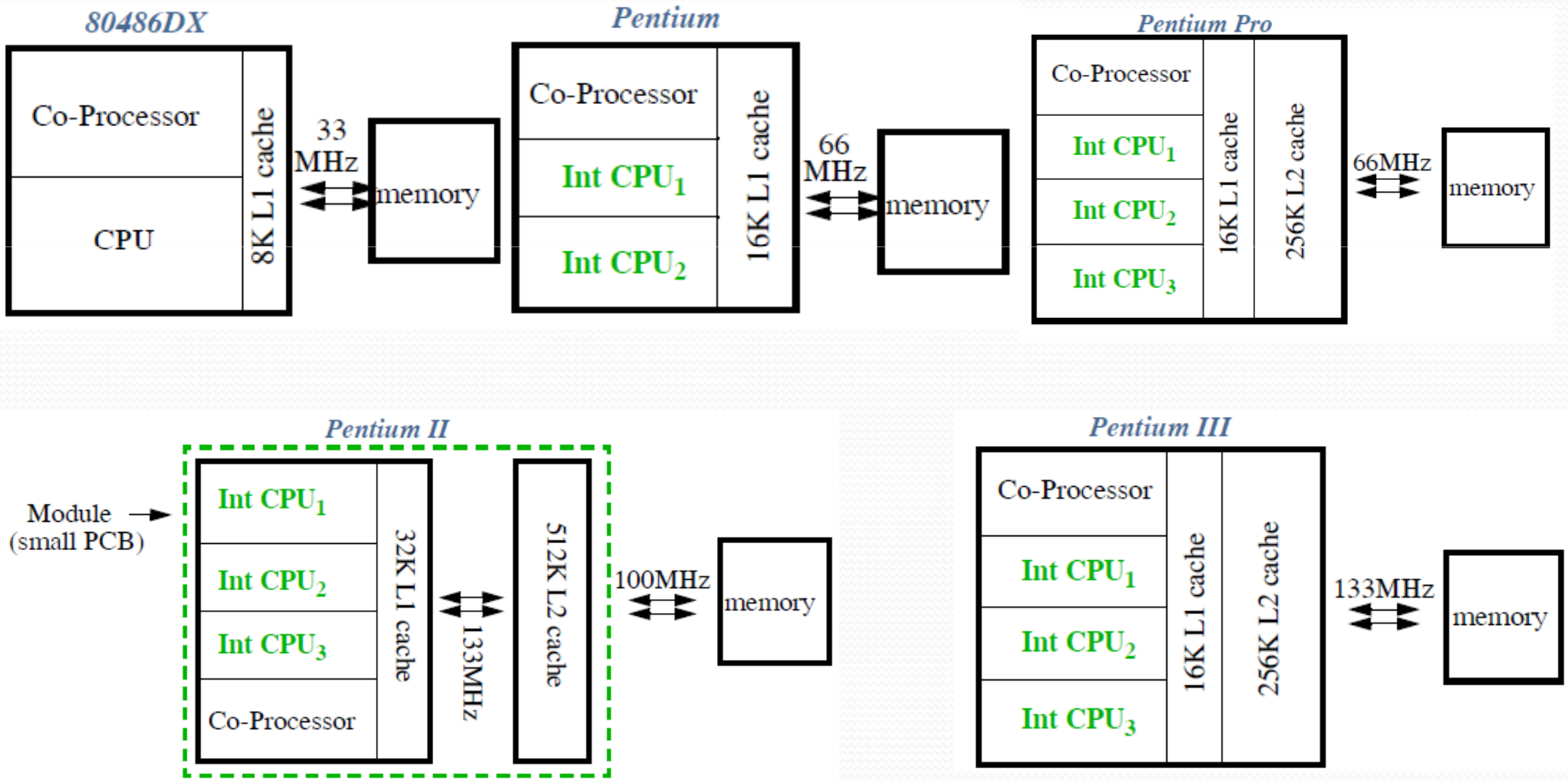
2010.2.21

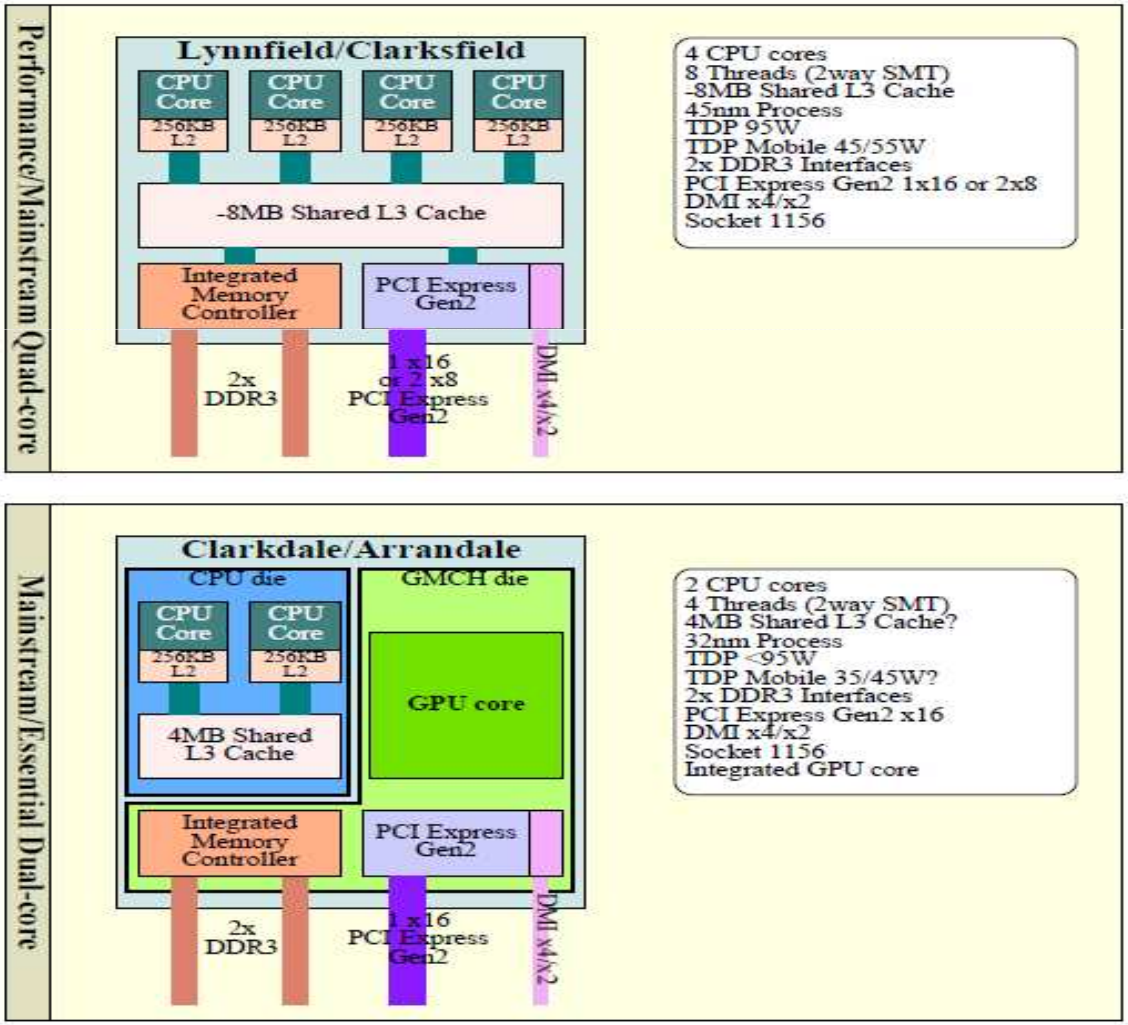
REMINDER 1: x86 Architecture (IA32)

- Basic Architecture unchanged since 1978 (8086)
  - CISC Architecture
  - 8 General Purpose Registers
    - EAX, EBX, ECX, EDX, EBP, ESP, ESI, EDI
  - 6 segment registers, processor status register, and an instruction pointer
- Instruction set:
  - One operand can be in memory
  - Variable instruction size (1 - 13 bytes)
  - Memory segmentation

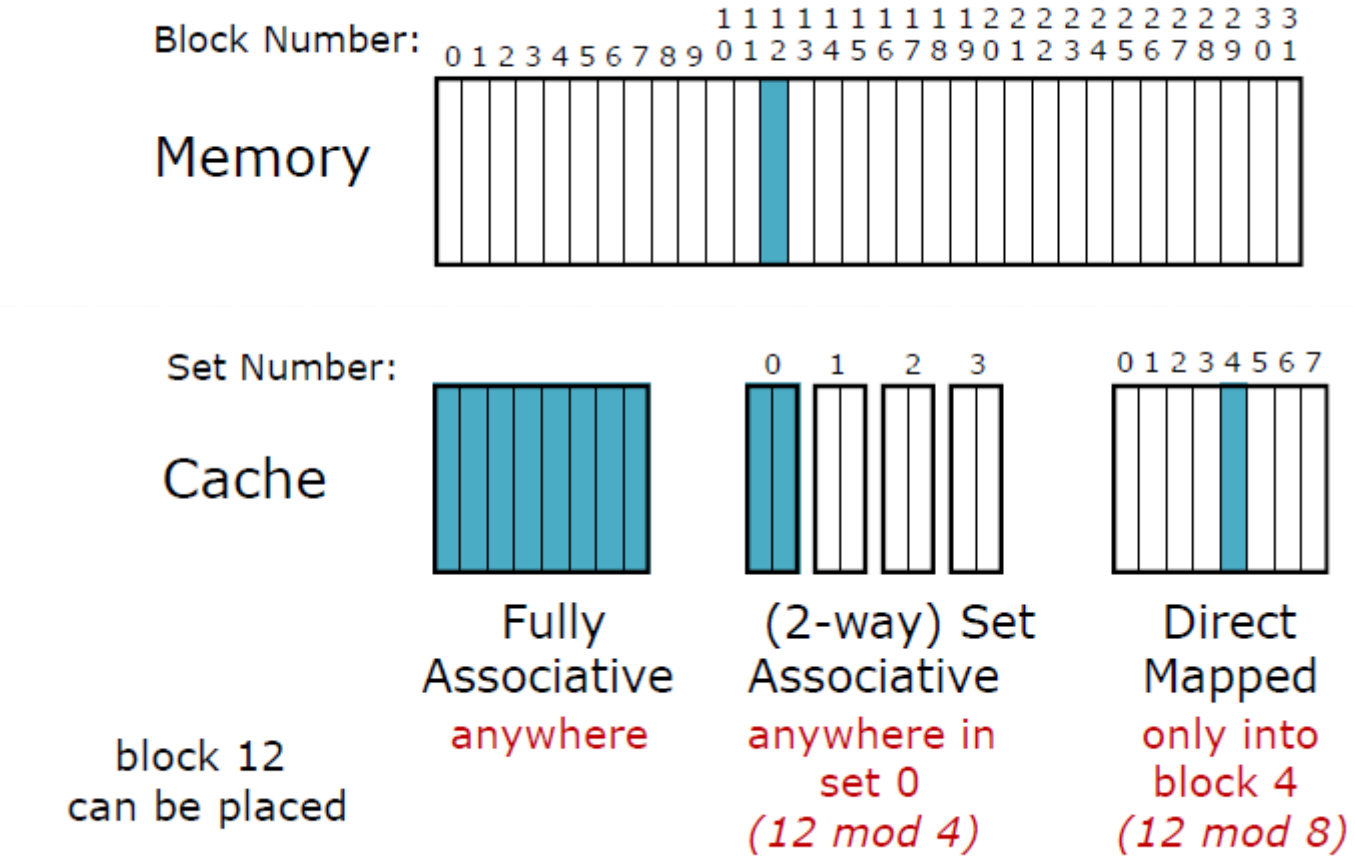
REMINDER 2: Recent History Cont.



REMINDER 3: Current Situation



REMINDER 4: Cache Organization



based on slides from CS152 Berkeley

REMINDER 5: Instruction Level Parallelism

- Pipelining
  - Instruction execution split into stages:
    - Fetch, Decode, Execude, Memory, Write back
  - Many instructions in execution at the same time
    - Just like a factory assembly line
- Superscalar
  - Multiple execution units:
    - 2 integer, 1 floating point, 1 logic
- SIMD (Single Instruction stream, Multible Data stream)
  - Data packed into data word, one instruction produces multiple results

Intel Architectures

- 8086
  - 16 bit
  - Since 8086 (8088 is similar with 8 bits external data bus)
  - 256K/1M memory (without, with segmentation)
  - 286 → Protected Mode
    - 16M memory
    - Virtual Memory
- IA32
  - 32 bit
  - Since 80386
  - 4G memory with Paging
  - Dynamic Execution
- Intel 64
  - 64 bit
  - Since 64 Bit Intel Xeon 3.6GHz

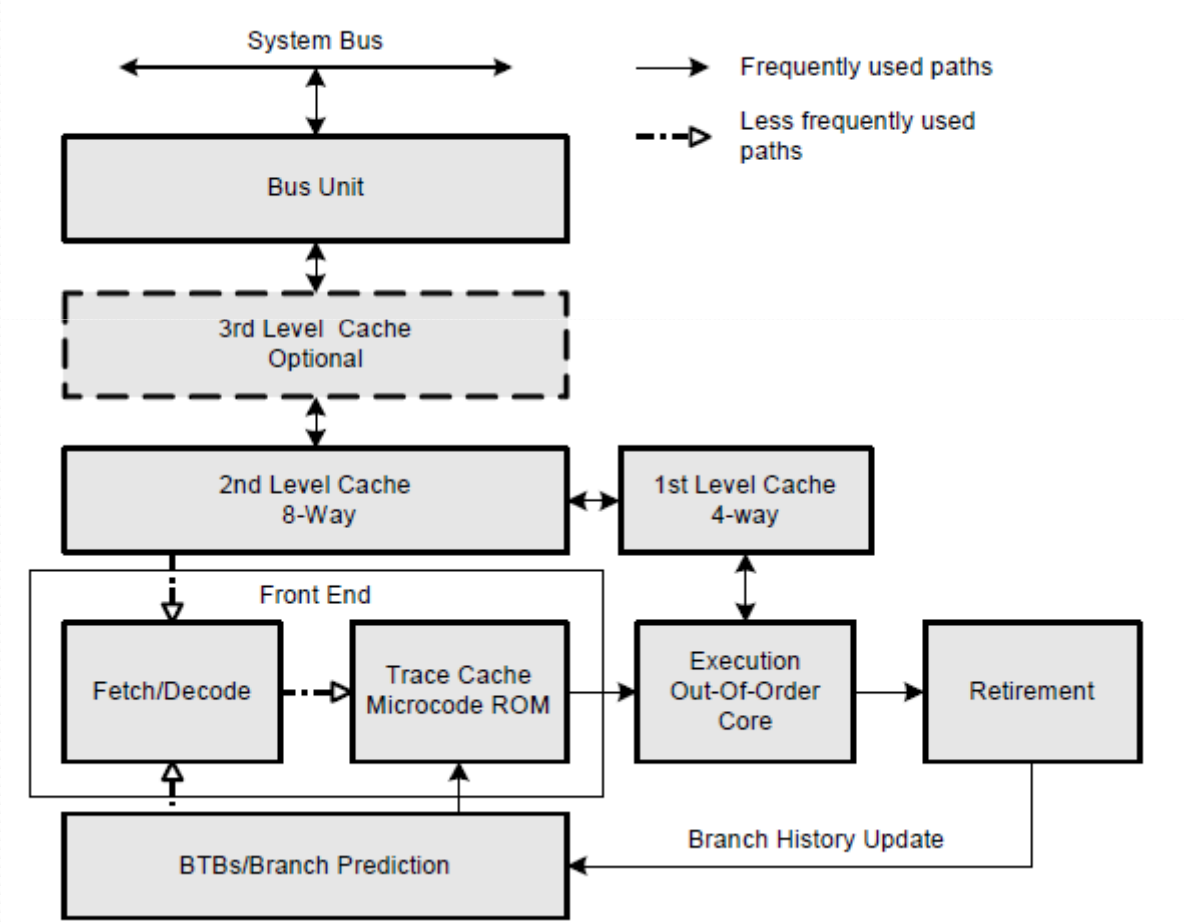
Dynamic Execution (P6 Family)

- Deep Branch Prediction
  - I know what will you do next
- Dynamic Data Flow Analysis
  - I know what will you use next
- Speculative Execution
  - I do not know what will you do next
  - Yet, I will execute more
  - Execution is not commitment!!
  - Uses DDFA and the *retirement* unit.

Intel NetBurst Architecture

- Rapid Execution (ALU at twice the cock)
- Deep Pipeline
- Deep out-of-order execution
  - Up to 126 instructions in flight
  - Up to 48 loads and 24 stores in pipeline
- Bus capable of providing 8.5GBytes bandwidth!!
- Register renaming

NetBurst


System Bus
Frequently used paths
Less frequently used paths
Bus Unit
3rd Level Cache
Optional
2nd Level Cache
8-Way
1st Level Cache
4-way
Front End
Fetch/Decode
Trace Cache
Microcode ROM
Execution
Out-Of-Order
Core
Retirement
BTBs/Branch Prediction
Branch History Update

Front End Pipeline

- Prefetchs instructions likely to be executed
- Decodes to microcodes
- Predicts branches

Out of Order Execution Core

- Dispatches up to 6 microcodes per cycle
- New microop at every cycle
- Integer operations → twice per cycle
- Floating Point operations → once per 2 cycles

Retirement Unit

- Receives results from out-of-order core
- Commits them to preserve original program's logic
- Up to 3 retired microops per cycle
- Keeps track of branches in Branch Target Buffer (BTB)

IA-32 Modes of Operation

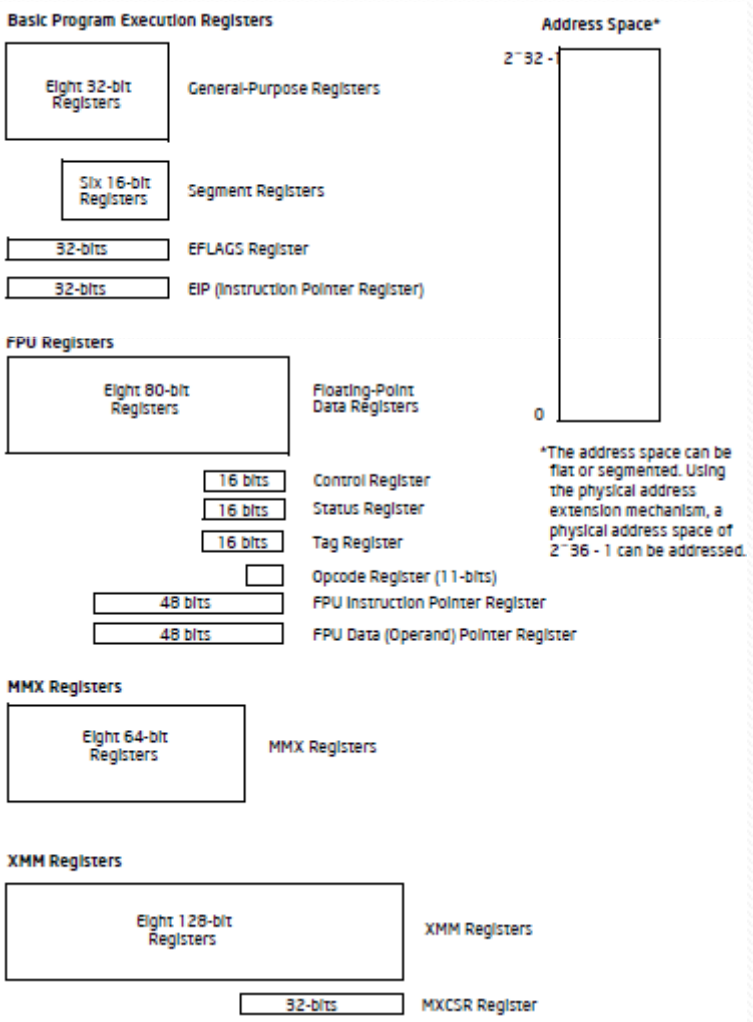
- Protected Mode
  - Native Mode
  - 4 Execution Privilege Levels
  - Supports Virtual 8086 mode
- Real Address Mode
  - 1M 8086 environment
  - Just after power-up
- System Management Mode (SMM)
  - External SMM interrupt bin is activated using APIC
  - Separate address space (saving old one)
  - Introduced in 386/486 SL
  - Used for power management and system security

Intel 64 modes

- IA-32e
  - Compatibility Mode
    - Most legacy 16 and 32 bit applications
    - Enabled by OS on a code segment basis
    - Similar to IA-32 Protected mode (up tp 4GB but extendable using PAE)
  - 64-bit mode
    - 64 bit Linear address space
    - 16 rather than 8 general purpose registers
    - Enabled by OS on a code segment basis
    - Default address is 64 bits and default operand is 32 bits

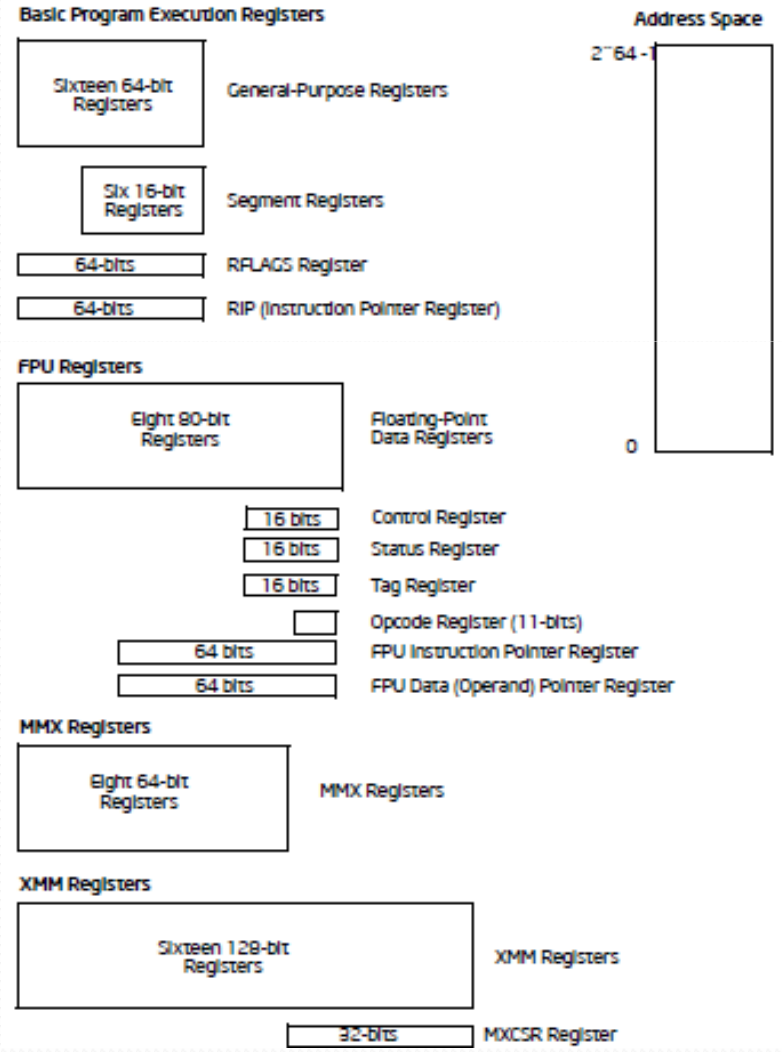
Execution Environment (IA-32)

- Address Space
  - IA-32 → Linear up to 4 GB and segmented up to 64 GB
- Basic Registers
  - 8 GPRs
  - EFLAGS, EIP
- X87 FPU Registers
  - 8 FPU data registers
  - FPU Control Register, Status Register
  - FPU Flag Register
  - …
- MMX Registers
  - 8 MMX Registers supporting SIMD on 64 bit data
- XMM Registers
  - 8 registers supporting SIMD on 128 bit values

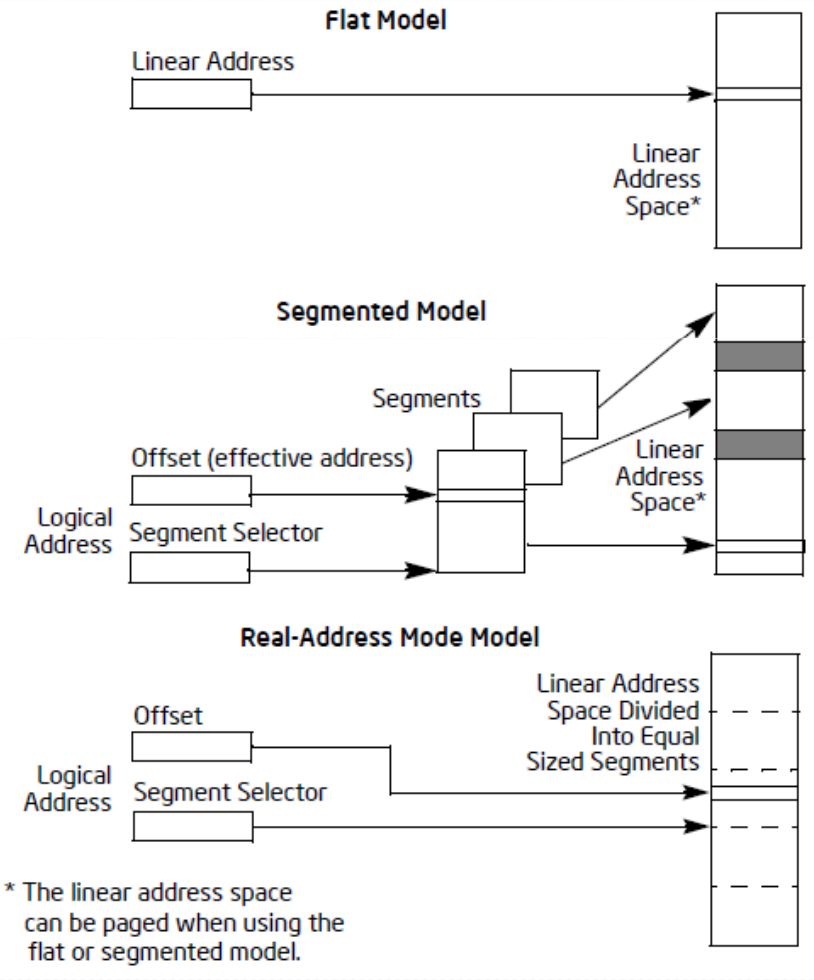


64-bit Execution Environment

- 16 GPRs (All 64)
- 64 bits EFLAGS (Upper 32 reserved)
- Up to 2^{64} linear memory
- 16 XMM registers



IA32 Memory Models



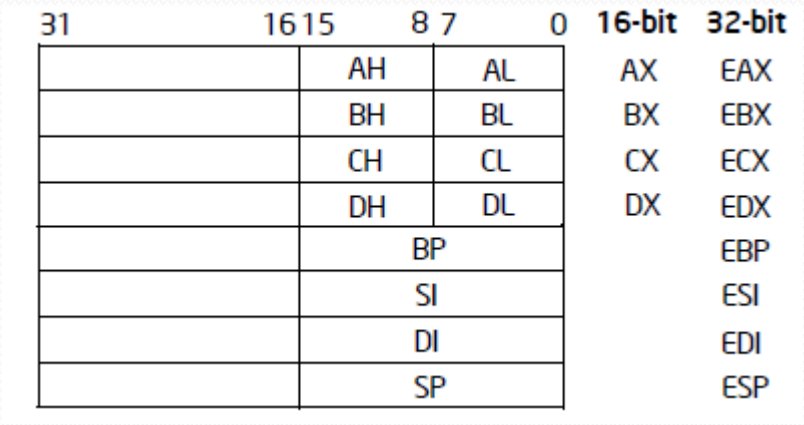
Operating and Memory Mode

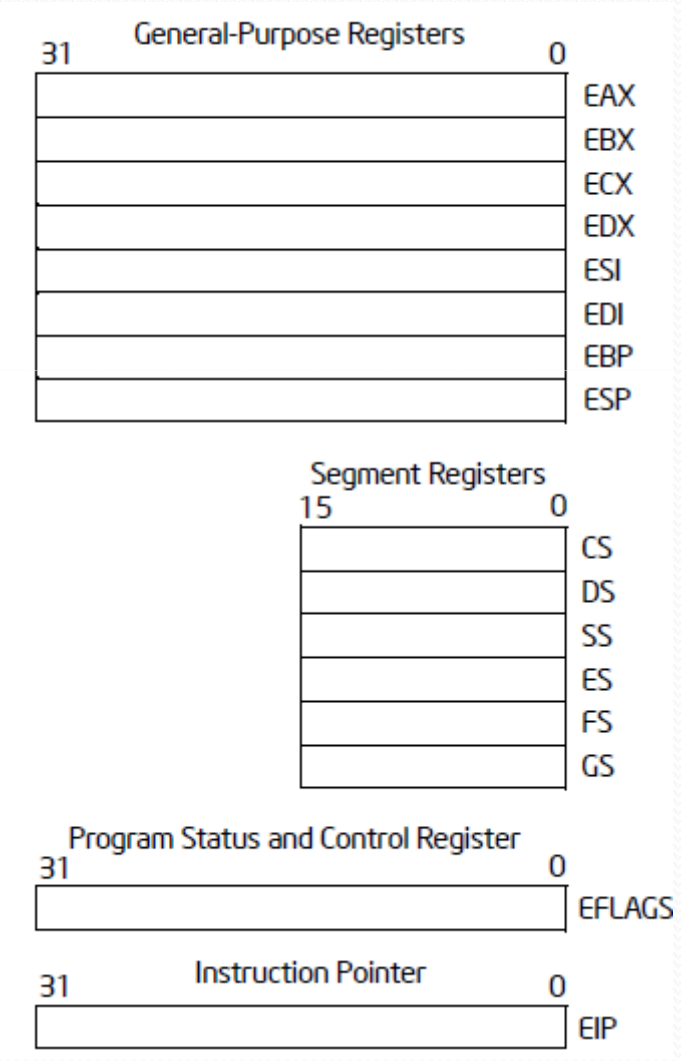
- Protected
  - All available (32 bits)
- Real-Address Mode
  - Only Flat with 16 Bit Registers
- SMM
  - Separate Read Address Space
- Compatibility Mode
  - All available (32 bits)
- 64-bit
  - Segmentation is usually Disabled

IP in different modes

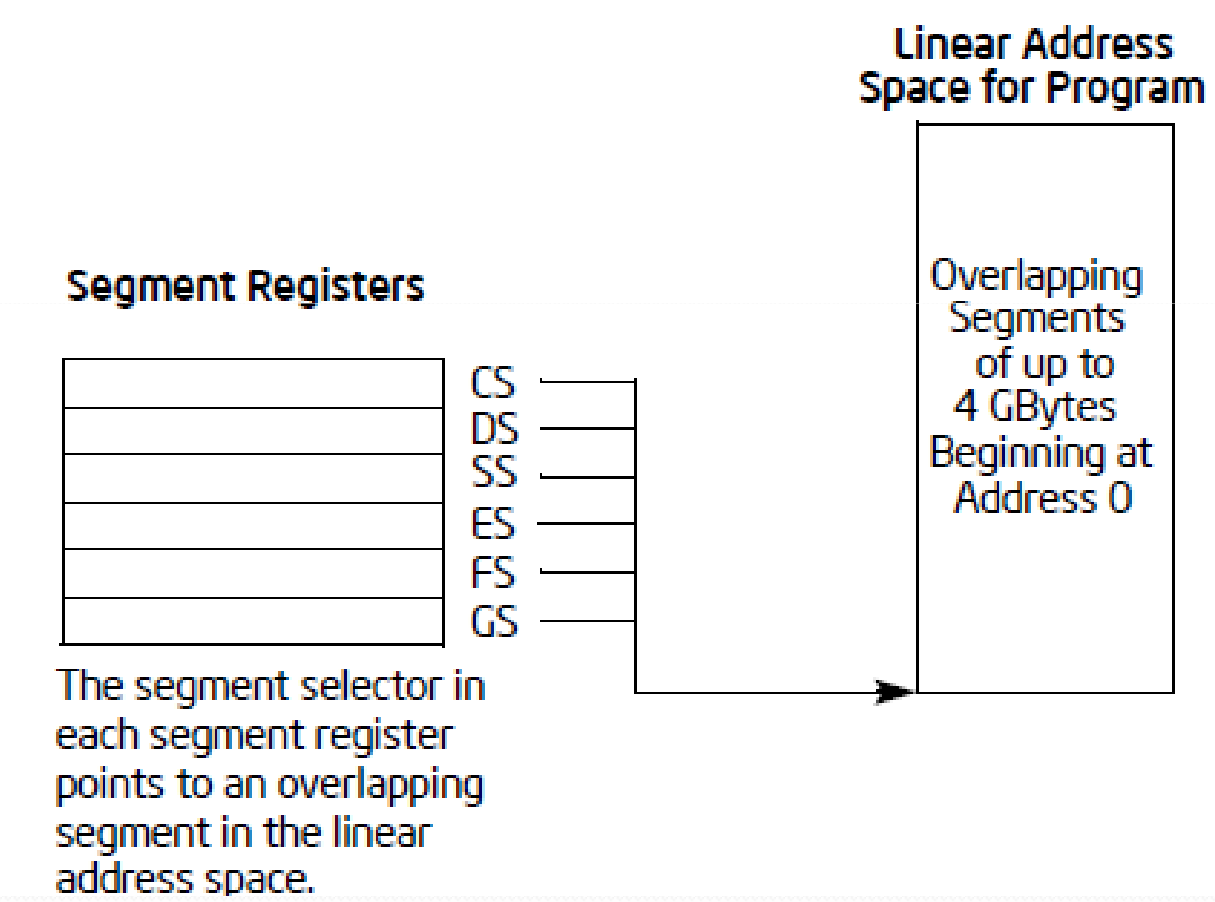
	Bits 63:32	Bits 31:16	Bits 15:0
16-bit instruction pointer	Not Modified		IP
32-bit instruction pointer	Zero Extension	EIP	
64-bit instruction pointer	RIP		

GPRs (32 bits)


31
16 15
8 7
0
16-bit
32-bit
AH
AL
AX
EAX
BH
BL
BX
EBX
CH
CL
CX
ECX
DH
DL
DX
EDX
BP
EBP
SI
ESI
DI
EDI
SP
ESP


General-Purpose Registers
31
0
EAX
EBX
ECX
EDX
ESI
EDI
EBP
ESP
Segment Registers
15
0
CS
DS
SS
ES
FS
GS
Program Status and Control Register
31
0
EFLAGS
Instruction Pointer
31
0
EIP

Use of Segment Registers Flat Memory



Use of Segment Registers Segmented Mode